Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
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HOWREY SIMON ARNOLD & WHITE, LLP
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Telephone: (650) 463-8100
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Attorneys for Defendants
AEROFLEX, INC.,
AMI SEMICONDUCTOR, INC.,
MATROX ELECTRONIC SYSTEMS LTD.,
MATROX GRAPHICS INC.,
MATROX INTERNATIONAL CORP., and
MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC., Defendants.	Case No. CO3-04669 MJJ **DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS** Date: May 4, 2004 Time: 9:30 a.m. Ctrm: 11, 19th Floor Judge: Hon. Martin J. Jenkins

I, Erik K. Moller, declare as follows:

1. I am an attorney at law licensed to practice in the State of California and an associate of the law firm of Howrey Simon Arnold & White, LLP, attorneys for defendants Aeroflex, Inc., AMI Semiconductor, Inc., Matrox Electronic Systems, Ltd., Matrox Graphics Inc., Matrox International Corp., and Matrox Tech, Inc. ("Defendants"). The matters set forth in this declaration are based upon my personal knowledge, except where otherwise indicated, and if called as a witness, I could and would testify competently thereto.

2. Attached hereto as Exhibit A is a true and correct copy of a later dated March 5, 2004, from Kenneth W. Brothers to Christopher Kelley.

3. Attached hereto as Exhibit B and submitted under seal is a true and correct copy of Ricoh's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("Aeroflex"), served on the Defendants by Ricoh on March 5, 2004.

4. Attached hereto as Exhibit C and submitted under seal is a true and correct copy of Ricoh's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("AMIS"), served on the Defendants by Ricoh on March 5, 2004.

5. Attached hereto as Exhibit D and submitted under seal is a true and correct copy of Ricoh's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("Matrox"), served on the Defendants by Ricoh on March 5, 2004.

6. Attached hereto as Exhibit E is a true and correct copy of a letter dated March 8, 2004, from Thomas C. Mavrakakis to Kenneth W. Brothers.

7. Attached hereto as Exhibit F is a true and correct copy of a letter dated March 12, 2004, from Eric Oliver to Thomas C. Mavrakakis.

8. Attached hereto as Exhibit G and submitted under seal is a true and correct copy of Ricoh's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("Aeroflex"), served on the Defendants by Ricoh on March 12, 2004.

9. Attached hereto as Exhibit H and submitted under seal is a true and correct copy of Ricoh's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("AMIS"), served on the Defendants by Ricoh on March 12, 2004.

10. Attached hereto as Exhibit I and submitted under seal is a true and correct copy of Ricoh's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("Matrox Electronics Systems, Ltd."), served on the Defendants by Ricoh on March 12, 2004.

11. Attached hereto as Exhibit J and submitted under seal is a true and correct copy of Ricoh's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("Matrox Graphics, Inc."), served on the Defendants by Ricoh on March 12, 2004.

12. Attached hereto as Exhibit K and submitted under seal is a true and correct copy of Ricoh's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("Matrox International Corp."), served on the Defendants by Ricoh on March 12, 2004.

13. Attached hereto as Exhibit L and submitted under seal is a true and correct copy of Ricoh's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("Matrox Tech, Inc."), served on the Defendants by Ricoh on March 12, 2004.

14. Attached hereto as Exhibit M is a true and correct copy of a letter dated March 16, 2004, from Thomas C. Mavrakakis to Kenneth W. Brothers.

15. Attached hereto as Exhibit N is a true and correct copy of a letter dated March 10, 2004 from Thomas C. Mavrakakis to Kenneth W. Brothers.

16. Attached hereto as Exhibit O is a true and correct copy of a letter dated March 12, 2004, from Thomas C. Mavrakakis to Kenneth W. Brothers.

17. Attached hereto as Exhibit P is a true and correct copy of a letter dated March 19, 2004, from Kenneth W. Brothers to Thomas C. Mavrakakis.

18. Attached hereto as Exhibit Q and submitted under seal is a true and correct copy of pages 1-9, 94-97, and 158-165 of the transcript of the deposition of Edward Dwyer, taken February 3, 2004.

19. Attached hereto as Exhibit R is a true and correct copy of an article by Ray Weiss, entitled, "Designers moving toward high-level logic representation via logic synthesis; Logic synthesis edging up design hierarchy," published in the February 6, 1989 issue of Electronic Engineering Times.

20. Attached hereto as Exhibit S is a true and correct copy of a response to an office action dated April 18, 1989, from the prosecution history of U.S. Patent No. 4,922,432.

21. Attached hereto as Exhibit T is a true and correct copy of an examiner interview summary record, dated October 19, 1989, from the prosecution history of U.S. Patent No. 4,922,432.

22. Attached hereto as Exhibit U is a true and correct copy of a response to an office action dated November 15, 1989, from the prosecution history of U.S. Patent No. 4,922,432.

Executed on March 30, 2004, in Menlo Park, California.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

/s/
Erik K. Moller

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW • Washington, DC 20037-1526
Tel (202) 785-9700 • Fax (202) 887-0689
Writer's Direct Dial: (202) 429-2184
E-Mail Address: BrothersK@dsmo.com

March 5, 2004

BY FACSIMILE AND U.S. MAIL
(650) 463-8400

Christopher Kelley, Esq.
Howrey Simon Arnold &White, LLP
301 Ravenswood Avenue
Menlo Park, CA 94025

Re: Ricoh v. Aeroflex et al.

Dear Chris:

Attached are Ricoh's disclosure of asserted claims and preliminary infringement contentions pursuant to Northern District of California Pat. L.R. 3-1. The attached charts are not intended to reference all potentially relevant supporting documents and discovery. Moreover, discovery in this case is on-going. Ricoh is in the process of reviewing discovery and documents that have been produced in connection with this litigation, and anticipates that additional documents and discovery will be produced by the parties in the future. Ricoh has already produced or has made available for inspection and copying the documents that are required to be produced pursuant to Pat. L.R. 3-2.

Pursuant to Pat. L.R. 3-3 and 3-4, the ASIC defendants are required to serve Ricoh with their preliminary invalidity contentions and supporting documents by no later than 45 days after today.

As we discussed today, you will consider these preliminary infringement charts in determining whether the parties might be able to reach a stipulation regarding the relevant similarities between the ASIC chips sold by the ASIC defendants.

Sincerely,

Kenneth W. Brothers

KWB/DA/bh
Enclosures

cc: Erik K. Moller, Esq. (w/enclosures)
Gary Hoffman, Esq.
Edward A. Meilman, Esq.
Jeffrey Demain, Esq.

FAX TRANSMISSION

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP

DATE: March 5, 2004

CLIENT NO.: R2180.0171

MESSAGE TO: Christopher Kelley
Erik K. Moller

COMPANY: Howrey Simon Arnold & White LLP

FAX NUMBER: (650) 463-8400

PHONE: (650) 463-8100

FROM: Kenneth W. Brothers

PHONE: (202) 429-2184

PAGES (Including Cover Sheet): 43 **HARD COPY TO FOLLOW:** X **YES** ____ **NO**

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Christopher Kelley (SBN 166608)
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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiffs, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.	Case No. CV 03-04669 MJJ(EMC) **MANUAL FILING NOTIFICATION** **RE EXHIBIT B TO DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS**

MANUAL FILING NOTIFICATION

Regarding: *Exhibit B to Declaration of Erik K. Moller in Support of Defendants' Motion To Strike Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions.*

This filing is in paper or physical form only, and is being maintained in the case file in the Clerk's office.

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___ Conformance with the Judicial Conference Privacy Policy (General Order 53).

___ Other (description): _____

Dated: March 30, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Erik K. Moller
Erik K. Moller
Attorneys for Defendants
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL COPR. and MATROX TECH, INC.

Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 147674)
Erik K. Moller (SBN 177927)
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Attorneys for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiffs, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.	Case No. CV 03-04669 MJJ(EMC) **MANUAL FILING NOTIFICATION** **RE EXHIBIT C TO DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS**

MANUAL FILING NOTIFICATION

Regarding: *Exhibit C to Declaration of Erik K. Moller in Support of Defendants' Motion To Strike Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions.*

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Dated: March 30, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Erik K. Moller
Erik K. Moller
Attorneys for Defendants
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL COPR. and MATROX TECH, INC.

Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 147674)
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Attorneys for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiffs, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.	Case No. CV 03-04669 MJJ(EMC) **MANUAL FILING NOTIFICATION** **RE EXHIBIT D TO DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS**

MANUAL FILING NOTIFICATION

Regarding: *Exhibit D to Declaration of Erik K. Moller in Support of Defendants' Motion To Strike Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions.*

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___ Other (description): _____

Dated: March 30, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Erik K. Moller
Erik K. Moller
Attorneys for Defendants
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL COPR. and MATROX TECH, INC.

HOWREY SIMON ARNOLD & WHITE HOWREY LLP ATTORNEYS AT LAW

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THOMAS C. MAVRAKAKIS
PARTNER
650.463.8169
mavrakakist@howrey.com

March 8, 2004

VIA FACSIMILE AND U.S. MAIL

Kenneth W. Brothers
Dickstein Shapiro Morin & Oshinsky, LLP
2101 L Street NW
Washington, D.C. 20037

Re: *Ricoh Company, Ltd. v. Aeroflex, Inc., et al.*,
Case No. CV 03-04669 MJJ (MCC)

Dear Mr. Brothers:

I am writing regarding the deficiencies in Ricoh's Patent Local Rule ("PLR") disclosures and accompanying document production. Ricoh's provision of a chart presumably under PLR 3-1(c) for only a few of the Defendants in the present action does not comply with the separate required identifications of the remainder of that PLR.

First, Ricoh has failed to comply with PLR 3-1(a), which requires the identification of "[e]ach claim of each patent in suit that is allegedly infringed by each opposing party." (emphasis added). Ricoh has not provided the required list identifying the claims of the '432 patent allegedly infringed by each Defendant. Until Ricoh's complies with PLR 3-1(a) its purported disclosures are ineffective.

Second, Ricoh has failed to comply with PLR 3-1(b), which requires Ricoh to identify: "Separately for each asserted claim, each...Accused Instrumentality of each opposing party." Aside from the impropriety of Ricoh's provision of a single chart for the four Matrox entities, Ricoh has also not provided the required list identifying the Accused Instrumentalities of each of the Defendants for each of the asserted '432 patent claims. Under this PLR, for each Defendant there must be an identification by Ricoh of the Accused Instrumentalities and the claims of the '432 patent alleged to have been infringed by them. Until Ricoh's complies with PLR 3-1(b) its purported disclosures are ineffective.

Third, Ricoh has failed to comply with PLR 3-1(c), because it has failed to provide a chart for each of the Defendants. Aside from Ricoh's failure to provide a chart for each of the Matrox entities that it has brought an infringement claim against, the chart required by PLR 3-1(c) requires identifying "where each element of each asserted claim is found within each Accused Instrumentality." Ricoh's chart is completely deficient. To comply, Ricoh must first identify the Accused Instrumentalities under PLR 3-1(b) and then for each of those provide a chart that complies with PLR 3-1(c). A chart must be provided for each Accused Instrumentality

HOWREY LLP
ATTORNEYS AT LAW

identified by Ricoh for each Defendant. Until Ricoh's complies with PLR 3-1(c) its purported disclosures are ineffective.

Similarly, Ricoh's failures to properly identify the Accused Instrumentalities under PLR 3-1(b) also render its attempted compliance with PLR 3-1(d) deficient as well.

With respect to PLR 3-1(f), we note Ricoh's failure to identify any of Ricoh's or its predecessor(s)-in-interest's instrumentalities that have allegedly practiced or practice the claimed invention. We understand that failure by Ricoh to be an intentional waiver by Ricoh of the right to rely on any such instrumentalities for any purpose in the pending litigations.

Next, Ricoh's document production under PLR 3-2 is equally deficient. PLR 3-2 requires that Ricoh "shall separately identify by production number which documents correspond to each category." Ricoh has not even attempted to comply with this requirement rendering its purported disclosures ineffective. Besides this failure, the Defendants demand that a copy of any of the documents within the categories set forth in PLR 3-2 be produced immediately.

Finally, to the extent Ricoh has been relying (albeit inappropriately) on PLR 2-5 to withhold any information responsive to any of Synopsys' Interrogatories (e.g., 1-3 and 6) in the *Synopsys, Inc. v. Ricoh Co., Ltd.* matter, that information should have been served contemporaneously with Ricoh's disclosures here. Synopsys demands that any such improperly withheld information be provided by no later than tomorrow, March 9, 2004.

At this time, the Defendants intend to move to strike Ricoh's inadequate PLR disclosures. We are available for an in-person meet and confer regarding these deficiencies in Ricoh's PLR disclosures and accompanying document production in accordance with Magistrate Judge Chen's Standing Order. Please suggest a time this week when your local counsel will be available to come to our Menlo Park Offices.

We look forward to your prompt response.

Very truly yours,

Thomas C. Mavrakakis/gj

Thomas C. Mavrakakis

TCM:gj

cc: Edward A. Meilman
Gary M. Hoffman

* * * COMMUNICATION RESULT REPORT (MAR. 8. 2004 2:47PM) * * *

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MENLO PARK, CA 94025-3434
PHONE: 650.463.8100 • FAX: 650.463.8400

FACSIMILE COVER SHEET

DATE: March 8, 2004

TO:

1. NAME: Kenneth Brothers and Gary M. Hoffman COMPANY: Dickstein Shapiro, et al.
   CITY: Washington, DC FAX #: (202) 887-0689 PHONE #: (202) 785-9700
2. NAME: Edward A. Meilman COMPANY: Dickstein Shapiro, et al.
   CITY: New York, NY FAX #: (212) 997-9880 PHONE #: (212) 835-1400
3. NAME: COMPANY:
   CITY: FAX #: PHONE #:
4. NAME: COMPANY:
   CITY: FAX #: PHONE #:
5. NAME: COMPANY:
   CITY: FAX #: PHONE #:

FROM: NAME: Thomas C. Mavrakakis

DIRECT DIAL NUMBER: (650) 463-8169 USER ID: 5229

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DATE: March 8, 2004

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DATE: March 8, 2004

TO:

1. NAME: Kenneth Brothers and Gary M. Hoffman COMPANY: Dickstein Shapiro, et al.
   CITY: Washington, DC FAX #: (202) 887-0689 PHONE #: (202) 785-9700
2. NAME: Edward A. Meilman COMPANY: Dickstein Shapiro, et al.
   CITY: New York, NY FAX #: (212) 997-9880 PHONE #: (212) 835-1400
3. NAME: COMPANY:
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4. NAME: COMPANY:
   CITY: FAX #: PHONE #:
5. NAME: COMPANY:
   CITY: FAX #: PHONE #:

FROM: NAME: Thomas C. Mavrakakis

DIRECT DIAL NUMBER: (650) 463-8169 USER ID: 5229

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March 12, 2004

VIA FACSIMILE AND FEDEX
1-650-463-8400

Thomas C. Mavrakakis, Esq.
Howrey Simon Arnold & White
301 Ravenswood Avenue
Menlo Park, CA 94025-3434

Re: Ricoh v. Aeroflex et al.

Dear Thomas:

We have reviewed your letter of March 4, 8 and 10, 2004. Although we do not agree with the various allegations you have raised, in order to avoid unnecessary controversy, we have reviewed and addressed your allegations regarding certain deficiencies in Ricoh's Preliminary Infringement Claim Charts as follows.

With respect to Patent Local Rule (PLR) 3-1(a), we believe that the original claim charts are in compliance. Nevertheless, we enclose revised claim charts separately identifying the different defendants, particularly the Matrox entities. We are willing to reset the effective date of disclosures to the date of this letter, if you find it necessary.

With respect to PLR 3-1(b), no change is necessary in the claim charts. As you will see upon reviewing the charts, the required identification of an "Accused Instrumentality" under the rule is met by the identification in the charts of the process carried out by the ASIC defendants, including the use of various software components identified in the charts.

With respect to PLR 3-1(c), the original claim charts had already set forth for each defendant the Accused Instrumentality, as noted above. Certainly, with the addition of the new claim charts separately identifying the Matrox entities, this objection has been rendered moot.

With respect to PLR 3-1(d), the original claim charts, together with the new Matrox claim charts, more than suffice to overcome your objection.

With respect to PLR 3-1(f), Ricoh identifies the following instrumentalities solely to preserve the right to rely (for any purpose) on such instrumentalities: the early implementations and variations of the KBSC system; and Ricoh's use of Synopsys products such as Design Compiler (or variation, e.g., DC Ultra, DC Expert, DC Expert

Plus, etc.), DFT Compiler, Prime Time, HDL Compiler for Verilog, Astro, Astro-Rail, and Astro-Xtalk.

With respect to PLR 3-2, Ricoh has no documents in category (a); Ricoh has already produced documents in category (b) (see production Nos. RCL002667 through RCL002693); and Ricoh has already produced the file history of the '432 patent (see production Nos. RCL000001 through RCL000265) required of category (c).

With respect to your letter of March 10th, Ricoh has met the claim chart disclosure requirements of PLR 3-1. Ricoh's preliminary claim charts set forth its theories of infringement with sufficient specificity. See Network Caching Technology, LLC v. Novel, Inc., 2003 U.S. Dist. Lexis 9881, *12-13 (N.D. Cal. 2003) (stating that "a party may comply with Patent LR 3-1 by setting forth particular theories of infringement with sufficient specificity to provide defendants' with notice of infringement beyond that which is provided by the mere language of the patents themselves").

Ricoh objects to the ASIC Defendants' attempt to turn the preliminary claim charts into a forum for litigation of the substantive issues. Such tactics are contrary to the Northern District of California's stated purpose of claim charts under PLR 3-1. *Id.* (finding that PLR 3-1 does not require the patentee produce evidence of infringement or ironclad and irrefutable claim constructions; the preliminary infringement contentions are not meant to be a forum for litigation of the substantive issues).

To the extent the ASIC Defendants take the position that Ricoh has not met its obligations under Fed. R. Civ. P. 11, this position is inconsistent with the present facts and the applicable case law. Ricoh has previously made clear that it conducted a good faith infringement analysis and, as such, has met the requirements of Rule 11 that you appear to complain about. See Q-Pharma, Inc. v. The Andrew Jergens Company, No. 03-1184, (Fed. Cir. Mar. 8, 2004) (applying Ninth Circuit law and noting that a Rule 11 violation does not exist merely because the accused disagrees with the patentee's infringement analysis, and further finding that "an infringement analysis can simply consist of a good faith, informed comparison of the claims of a patent against the accused subject matter"). Ricoh has met its burden here.

With respect to the response to interrogatories served in the Synopsys, Inc. v. Ricoh Co., Ltd. litigation (" Synopsys litigation"), which issue was also raised in your letter of March 4, 2004,[1] we note that the Synopsys litigation is a separate case that has not been consolidated with the Ricoh Co., Ltd. v. Aeroflex et al. litigation ("Ricoh litigation"). As such, the disclosure of the Preliminary Infringement Charts in the Ricoh litigation does not obligate us to supplement our responses to interrogatories served in the Synopsys litigation. Nevertheless, we will review the issue and supplement our responses if appropriate.

[1] We note that you had failed to timely object to our position on the issue as previously set forth in the letters from Edward Meilman on December 17th and 19th, 2003.

We believe that we have addressed all outstanding issues raised in your letters of March 4, 8 and 10, 2004. To the extent there are any other issues that have not been specifically addressed herein, we do not acquiesce to or otherwise agree with your position and recommend that you identify such remaining issues immediately so that they can be addressed at this time.

We are more than willing to schedule a meet and confer consistent with Judge Chen's directives on a mutually agreeable date and time in order to resolve any outstanding issues.

Very truly yours,

Erie Oliver

EO/cdl
Enclosures

FAX TRANSMISSION

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP

2004 MAR 12 PM 4:54

DATE: March 12, 2004

CLIENT NO.: R2180.0171

MESSAGE TO: Thomas C. Mavrakakis, Esq.

COMPANY: Howrey Simon Arnold & White

FAX NUMBER: 1-650-463-8400

PHONE:

FROM: Eric Oliver

PHONE: 202-861-9185

PAGES (Including Cover Sheet): _____ **HARD COPY TO FOLLOW:** x **YES** _____ **NO**

SENT BY:		DATE/TIME:	

MESSAGE:

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Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 147674)
Erik K. Moller (SBN 177927)
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Attorneys for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiffs, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.	Case No. CV 03-04669 MJJ(EMC) **MANUAL FILING NOTIFICATION** **RE EXHIBIT G TO DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS**

MANUAL FILING NOTIFICATION

Regarding: *Exhibit G to Declaration of Erik K. Moller in Support of Defendants' Motion To Strike Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions.*

This filing is in paper or physical form only, and is being maintained in the case file in the Clerk's office.

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___ Conformance with the Judicial Conference Privacy Policy (General Order 53).

___ Other (description): _____

Dated: March 30, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Erik K. Moller
Erik K. Moller
Attorneys for Defendants
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL COPR. and MATROX TECH, INC.

Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 147674)
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Attorneys for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiffs, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.	Case No. CV 03-04669 MJJ(EMC) **MANUAL FILING NOTIFICATION** **RE EXHIBIT H TO DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS**

MANUAL FILING NOTIFICATION

Regarding: *Exhibit H to Declaration of Erik K. Moller in Support of Defendants' Motion To Strike Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions.*

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___ Conformance with the Judicial Conference Privacy Policy (General Order 53).

___ Other (description): _____

Dated: March 30, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Erik K. Moller
Erik K. Moller
Attorneys for Defendants
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL COPR. and MATROX TECH, INC.

Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 147674)
Erik K. Moller (SBN 177927)
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Attorneys for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiffs, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.	Case No. CV 03-04669 MJJ(EMC) **MANUAL FILING NOTIFICATION** **RE EXHIBIT I TO DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS**

MANUAL FILING NOTIFICATION

Regarding: *Exhibit I to Declaration of Erik K. Moller in Support of Defendants' Motion To Strike Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions.*

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___ Conformance with the Judicial Conference Privacy Policy (General Order 53).

___ Other (description): _____

Dated: March 30, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Erik K. Moller
Erik K. Moller
Attorneys for Defendants
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL COPR. and MATROX TECH, INC.

Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 147674)
Erik K. Moller (SBN 177927)
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Attorneys for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiffs, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.	Case No. CV 03-04669 MJJ(EMC) **MANUAL FILING NOTIFICATION** **RE EXHIBIT J TO DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS**

MANUAL FILING NOTIFICATION

Regarding: *Exhibit J to Declaration of Erik K. Moller in Support of Defendants' Motion To Strike Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions.*

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___ Conformance with the Judicial Conference Privacy Policy (General Order 53).

___ Other (description): _____

Dated: March 30, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Erik K. Moller
Erik K. Moller
Attorneys for Defendants
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL COPR. and MATROX TECH, INC.

Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 147674)
Erik K. Moller (SBN 177927)
HOWREY SIMON ARNOLD & WHITE, LLP
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Attorneys for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiffs, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.	Case No. CV 03-04669 MJJ(EMC) **MANUAL FILING NOTIFICATION** **RE EXHIBIT K TO DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS**

MANUAL FILING NOTIFICATION

Regarding: *Exhibit K to Declaration of Erik K. Moller in Support of Defendants' Motion To Strike Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions.*

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___ Conformance with the Judicial Conference Privacy Policy (General Order 53).

___ Other (description): _____

Dated: March 30, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Erik K. Moller
Erik K. Moller
Attorneys for Defendants
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL COPR. and MATROX TECH, INC.

Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 147674)
Erik K. Moller (SBN 177927)
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Attorneys for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiffs, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.	Case No. CV 03-04669 MJJ(EMC) **MANUAL FILING NOTIFICATION** **RE EXHIBIT L TO DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS**

MANUAL FILING NOTIFICATION

Regarding: *Exhibit L to Declaration of Erik K. Moller in Support of Defendants' Motion To Strike Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions.*

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___ Conformance with the Judicial Conference Privacy Policy (General Order 53).

___ Other (description): _____

Dated: March 30, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Erik K. Moller
Erik K. Moller
Attorneys for Defendants
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL COPR. and MATROX TECH, INC.

HOWREY SIMON ARNOLD & WHITE HOWREY LLP ATTORNEYS AT LAW

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THOMAS C. MAVRAKAKIS
PARTNER
650.463.8169
mavrakakist@howrey.com

March 16, 2004

VIA FACSIMILE AND U.S. MAIL

Kenneth W. Brothers
Dickstein Shapiro Morin & Oshinsky, LLP
2101 L Street NW
Washington, D.C. 20037

Re: *Ricoh Company, Ltd. v. Aeroflex, Inc., et al.*,
Case No. CV 03-04669 MJJ (MCC)

Dear Mr. Brothers:

The Defendants object to Ricoh's provision of so-called "revised claim charts" purportedly under Patent Local Rule ("PLR") 3-1. PLR 3-7 prohibits Ricoh from modifying or amending its original PLR 3-1 disclosures absent an order from the Court, which must be based on Ricoh's establishing "good cause" for such modifications or amendments.

Ricoh's failure to provide any disclosure under PLR 3-1(f) in its original PLR 3-1 disclosure waived its right to rely on any such instrumentalities for any purpose in this litigation. Ricoh's belated attempt to make such a disclosure in Mr. Oliver's March 12, 2004 letter is not only ineffective but still fails to comply PLR 3-1(f)'s requirement that the identification of Ricoh's instrumentalities "practic[ing] the claimed invention" be done "separately for each asserted claim." Similarly, Ricoh's failure to timely identify the categories of documents pursuant to PLR 3-2(b) has waived its right to rely on any documents under those categories, including those documents untimely identified in Mr. Oliver's letter (i.e., production Nos. RCL002667-2693). Based on these failures, the Defendants will seek to preclude Ricoh from relying on any instrumentalities under PLR 3-1(f) as well as any evidence under PLR 3-2(b) in the present action.

Aside from the fact that Ricoh's "revised claim charts" violate PLR 3-7, they remain inadequate under PLR 3-1. The purpose of PLR 3-1 is for Ricoh to "crystallize its theory of the case." Instead, Ricoh's original charts and revised charts leave the Defendants to guess at, among other things, what are the accused instrumentalities which "when used allegedly results in the practice of the claimed method or process."

PLR 3-1(a) requires Ricoh to affirmatively identify each claim allegedly infringed by each of the Defendants. Ricoh's original chart did not comply. Ricoh's revised chart appears to show that Ricoh believes that claims 13-17 are allegedly infringed by each of the Defendants. But the Defendants are not required to guess about or interpret what Ricoh's charts provide and there is simply no excuse for Ricoh's failure to explicitly state which of the '432 patent claims it alleges each Defendant infringes. The Defendants are entitled to a clear and unambiguous statement of what claims they are alleged to have infringed.

HOWREY SIMON ARNOLD & WHITE HOWREY LLP ATTORNEYS AT LAW

PLR 3-1(b) requires Ricoh for each Defendant to identify "[s]eparately for each claim" each accused instrumentality which "when used allegedly results in the practice of the claimed method or process." Thus, for each Defendant and for each of the claims identified pursuant to PLR 3-1(a), Ricoh must identify "as specific as possible" the products and their version numbers that when used by each of the Defendants allegedly practice the claimed process of that particular claim. Ricoh's original and revised charts fail to comply with these requirements.

Instead, Ricoh's charts leave the Defendants to guess at what the products are which allegedly infringe each of the claims by broadly defining terms such as "Design Compiler Family", "HDL Compiler Family", and "Synopsys Design Tools" in footnotes 2-5. This listing of numerous products and use of phrases such as "without limitation", "etc", and "include at least" by Ricoh is an attempt by Ricoh to avoid providing the identification required by PLR 3-1(b). Specifically, both Ricoh's original and revised charts fail to identify which of the products listed in the footnotes allegedly practice the claimed process for any of the '432 patent claims. Moreover, Ricoh's use of the phrases "without limitation", "etc", "include at least" and its statement that it reserves the right (which the PLRs make clear it does not have) to add an infringement analysis to one or more additional "Synopsys Design Tools" are improper and should be removed. Ricoh also fails to identify a single version number for any products listed in footnotes 2-5.

PLR 3-1(c) requires Ricoh to provide a separate chart for each product (accused instrumentality) identified pursuant to PLR 3-1(b). As noted above, Ricoh's revised and original charts seek to avoid this requirement by listing numerous products in the footnotes under broad terms such as "Design Compiler Family", "HDL Compiler Family", and "Synopsys Design Tools." This does not comply with PLR 3-1(c) since Ricoh was required to provide a chart for each product it wishes to pursue infringement on in the present action.

PLR 3-1(c) also requires identifying where each element of each claim is found within each product ("Accused Instrumentality"). This requires that Ricoh explain how the product materials or other information about the accused products it bases its claims on map onto the corresponding claim language of the particular element of the claims. Ricoh has not done this. Consequently, not only do Ricoh's charts fail to separately address each product but they also are lacking substantively since they fail to comply with the identifying where each element of each claim is found within each product requirement as well.

Finally, Ricoh has not identified whether each element of each claim is literally present or present under the doctrine of equivalents for each product (accused instrumentality) as required by PLR 3-1(d). Consequently, based on this and its failures under the remainder of PLR 3-1, Ricoh has waived its right to claim infringement with respect to such products. *See Genentech, Inc. v. Amgen, Inc.*, 289 F.3d 761 (Fed. Cir. 2002).

HOWREY LLP
ATTORNEYS AT LAW

We remain willing to consider any amended PLR 3-1 disclosures that address the inadequacies identified above that Ricoh provides prior to our scheduled meet and confer on these issues on March 17, 2004.

Very truly yours,

Thomas C. Mavrakakis

TCM:bal
cc: Edward A. Meilman
Gary M. Hoffman

MEMORY TRANSMISSION REPORT

TIME : MAR-16-2004 02:23PM
TEL NUMBER : 650-463-8400
NAME : HOWREY

FILE NUMBER : 657
DATE : MAR-16 02:19PM
TO : 2#734#912028870689#
DOCUMENT PAGES : 004
START TIME : MAR-16 02:19PM
END TIME : MAR-16 02:23PM
SENT PAGES : 004
STATUS : OK
FILE NUMBER : 657

*** SUCCESSFUL TX NOTICE ***

HOWREY LLP
WHERE LEADERS GO

301 RAVENSWOOD AVENUE
MENLO PARK, CA 94025-3434
PHONE: 650.463.8100 • FAX: 650.463.8400

FACSIMILE COVER SHEET

DATE: March 16, 2004
TO:
1. NAME: _____ COMPANY: _____
CITY: _____ FAX #: _____ PHONE #: _____
2. NAME: Gary M. Hoffman and Kenneth Brothers COMPANY: Dickstein Shapiro, et al.
CITY: Washington, DC FAX #: (202) 887-0689 PHONE #: (202) 785-9700
3. NAME: Edward A. Meilman COMPANY: Dickstein Shapiro, et al.
CITY: New York, NY FAX #: (212) 997-9880 PHONE #: (212) 835-1400
4. NAME: _____ COMPANY: _____
CITY: _____ FAX #: _____ PHONE #: _____
5. NAME: _____ COMPANY: _____
CITY: _____ FAX #: _____ PHONE #: _____

FROM: NAME: Thomas C. Mavrakakis, Esq.
DIRECT DIAL NUMBER: (650) 463-8169 USER ID: 5229
NUMBER OF PAGES, INCLUDING COVER: 4 CHARGE NUMBER: 06816.0060.000000

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MEMORY TRANSMISSION REPORT

TIME : MAR-16-2004 02:25PM
TEL NUMBER : 650-463-8400
NAME : HOWREY

FILE NUMBER : 658

DATE : MAR-16 02:20PM

TO : 2#354#912129979880#

DOCUMENT PAGES : 004

START TIME : MAR-16 02:23PM

END TIME : MAR-16 02:25PM

SENT PAGES : 004

STATUS : OK

FILE NUMBER : 658 *** SUCCESSFUL TX NOTICE ***

HOWREY LLP
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PHONE: 650.463.8100 • FAX: 650.463.8400

FACSIMILE COVER SHEET

DATE: March 16, 2004

TO:

1. NAME: _____ COMPANY: _____
CITY: _____ FAX #: _____ PHONE #: _____

2. NAME: Gary M. Hoffman and Kenneth Brothers COMPANY: Dickstein Shapiro, et al.
CITY: Washington, DC FAX #: (202) 887-0689 PHONE #: (202) 785-9700

3. NAME: Edward A. Meilman COMPANY: Dickstein Shapiro, et al.
CITY: New York, NY FAX #: (212) 997-9880 PHONE #: (212) 835-1400

4. NAME: _____ COMPANY: _____
CITY: _____ FAX #: _____ PHONE #: _____

5. NAME: _____ COMPANY: _____
CITY: _____ FAX #: _____ PHONE #: _____

FROM: NAME: Thomas C. Mavrakakis, Esq.
DIRECT DIAL NUMBER: (650) 463-8169 USER ID: 5229
NUMBER OF PAGES, INCLUDING COVER: 4 CHARGE NUMBER: 06816.0060.000000

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SUPPLEMENTAL MESSAGE:
Sent via fax and first class mail is my letter to you dated 3/16/04.

HOWREY SIMON ARNOLD & WHITE HOWREY LLP WHERE LEADERS GO™

301 RAVENSWOOD AVENUE
MENLO PARK, CA 94025-3434
PHONE: 650.463.8100 • FAX: 650.463.8400

FACSIMILE COVER SHEET

DATE: March 16, 2004

TO:

1. NAME: _____ COMPANY: _____
   CITY: _____ FAX #: _____ PHONE #: _____
2. NAME: Gary M. Hoffman and Kenneth Brothers COMPANY: Dickstein Shapiro, et al.
   CITY: Washington, DC FAX #: (202) 887-0689 PHONE #: (202) 785-9700
3. NAME: Edward A. Meilman COMPANY: Dickstein Shapiro, et al.
   CITY: New York, NY FAX #: (212) 997-9880 PHONE #: (212) 835-1400
4. NAME: _____ COMPANY: _____
   CITY: _____ FAX #: _____ PHONE #: _____
5. NAME: _____ COMPANY: _____
   CITY: _____ FAX #: _____ PHONE #: _____

FROM: NAME: Thomas C. Mavrakakis, Esq.

DIRECT DIAL NUMBER: (650) 463-8169 USER ID: 5229

NUMBER OF PAGES, INCLUDING COVER: 4 CHARGE NUMBER: 06816.0060.000000

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SUPPLEMENTAL MESSAGE:

Sent via fax and first class mail is my letter to you dated 3/16/04.

HOWREY SIMON ARNOLD & WHITE LLP
ATTORNEYS AT LAW

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PHONE 650.463.8100
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A LIMITED LIABILITY PARTNERSHIP

THOMAS C. MAVRAKAKIS
PARTNER
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mavrakakist@howrey.com

March 10, 2004

VIA FACSIMILE AND U.S. MAIL

Kenneth W. Brothers
Dickstein Shapiro Morin & Oshinsky, LLP
2101 L Street NW
Washington, D.C. 20037

Re: *Ricoh Company, Ltd. v. Aeroflex, Inc., et al.*,
Case No. CV 03-04669 MJJ (MCC)

Dear Mr. Brothers:

Ricoh's responses to Synopsys' Interrogatories, the Defendants' Interrogatories and Ricoh's purported Preliminary Infringement Contentions pursuant Patent Local Rule ("PLR") 3-1 confirm that Ricoh brought the instant litigation without any factual basis for believing that any of the Defendants have performed, among other things, the steps of: "storing in an expert system knowledge base a set of rules for selecting the hardware cells" and "selecting a hardware cell for performing the desired function of the ASIC through use of cell selection rules stored in the expert system knowledge base." In fact, Ricoh's recent purported PLR disclosure demonstrates that even now Ricoh has no basis for maintaining the present action against any of these Defendants.

Synopsys and each of the Defendants have suffered and continue to suffer damages as a result of Ricoh's threats against Synopsys' customers (including the Defendants), filing of the instant litigation against the Defendants, and continued prosecution of the instant litigation against the Defendants. If Ricoh believes that it has ever had any basis for the threats, allegations, and claims that any of the Defendants perform any of the steps claimed in the '432 patent (including the above-identified steps) by using Synopsys' software products then the Defendants and Synopsys demand that Ricoh provide the factual basis for any such belief by supplementing its interrogatory responses and/or its purported PLR disclosures by the end of the week to include any such factual basis. This information is not only required to be included in the PLR disclosures but it is also responsive to the interrogatories already served by the Defendants and Synopsys and therefore, should have been provided to them by Ricoh in its responses months ago.

We look forward to your prompt response.

Very truly yours,

Thomas C. Mavrakakis

TCM:bal
cc: Edward A. Meilman
Gary M. Hoffman

8010897

* * * COMMUNICATION RESULT REPORT (MAR. 10. 2004 10:15AM) * * *

FAX HEADER 1: HOWREY SIMON ARNOLD
FAX HEADER 2:

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DATE: March 10, 2004

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   CITY: New York, NY FAX #: (212) 997-9880 PHONE #: (212) 835-1400
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5. NAME: _____ COMPANY: _____
   CITY: _____ FAX #: _____ PHONE #: _____

FROM: NAME: Thomas C. Mavrakakis, Esq.

DIRECT DIAL NUMBER: (650) 463-8169 USER ID: 5229

NUMBER OF PAGES, INCLUDING COVER: 2 CHARGE NUMBER: 06816.0060.000000

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SUPPLEMENTAL MESSAGE:

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MENLO PARK, CA 94025-3434
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HOWREY SIMON ARNOLD & WHITE
HOWREY LLP
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March 12, 2004

VIA FACSIMILE AND U.S. MAIL

Kenneth W. Brothers
Dickstein Shapiro Morin & Oshinsky, LLP
2101 L Street NW
Washington, D.C. 20037

Re: *Ricoh Company, Ltd. v. Aeroflex, Inc., et al.*,
Case No. CV 03-04669 MJJ (MCC)

Dear Mr. Brothers:

Your March 12, 2004 letter not only fails to address any of the concerns raised in my letters regarding Ricoh's Patent Local Rule ("PLR") disclosures and its interrogatory responses but also fails to affirmatively commit to a meet and confer on those issues. We flatly reject your attempt to condition the meet and confer on these issues by raising wholly unrelated issues Ricoh has with the Defendants' discovery. We expect that you will participate in the requested meet and confers regarding Ricoh's purported PLR disclosures and inadequate responses to Synopsys' Interrogatories 1-3 and 6 by the end of the day on Wednesday, March 17, 2004.

With respect to Ricoh's attempt to thwart the very purpose of the PLRs with its inadequate PLR 3-1 disclosures and productions under PLR 3-2, the Defendants are not required to and will not be burdened while Ricoh makes numerous attempts to avoid the clear requirements of PLR 3-1 and 3-2. PLR 3-7 prohibits Ricoh from modifying or amending its PLR 3-1 disclosures absent an order from the Court, which must be based on Ricoh's establishing "good cause" for such modifications or amendments. Defendants do not believe that Ricoh can make such a showing and as an initial matter are not inclined to agree that Ricoh may make any modifications and amendments of Ricoh's disclosures. In fact, the Defendants believe that Ricoh has already waived, among other things, its rights under PLR3-1 to claim infringement literally and/or under the doctrine of equivalents on Accused Instrumentalities for which Ricoh has failed to comply with one or more of the requirements of the PLRs. The Defendants are, however, willing to consider any written proposed modified or amended PLR 3-1 disclosures and productions under PLR 3-2 and meet and confer with the Ricoh on this issue by the end of the day on Wednesday, March 17, 2004. Otherwise the Defendants will seek an order from the Court striking Ricoh's PLR disclosures.

Next, Ricoh's continued withholding of information responsive to Synopsys' Interrogatories 1-3 and 6 must end immediately. Ricoh (not Synopsys) has the burden of proving infringement on Synopsys' non-infringement declaratory judgment claim. Similarly, Ricoh has no basis for withholding the identification of claim language it believes distinguishes over the Darringer prior art patent relied on by the examiner in the file history of the '432 patent. We asked for the required meet and confer more than a week ago and still have not received any response. We will consider Ricoh's failure to unconditionally meet and confer regarding this issue by Wednesday, March 17, 2004 a refusal to meet and confer.

HOWREY LLP
ATTORNEYS AT LAW

Finally, we take your failure to respond substantively to my letter regarding the lack of a factual basis for Ricoh's threats and claims regarding infringement of the '432 patent as an admission that any factual basis Ricoh ever had for its threats and claims against Defendants' use of Synopsys' software products is limited to Ricoh's responses to Defendants' and Synopsys' Interrogatories as they stand today, March 12, 2004.

We look forward to your prompt response.

Very truly yours,

Thomas C. Mavrakakis

TCM:bal
cc: Edward A. Meilman
Gary M. Hoffman

* * * COMMUNICATION RESULT REPORT (MAR. 12. 2004 4:53PM) * * *

FAX HEADER 1: HOWREY SIMON ARNOLD
FAX HEADER 2:

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PHONE: 650.463.8100 • FAX: 650.463.8400

FACSIMILE COVER SHEET

DATE: March 12, 2004

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1. NAME: _____ COMPANY: _____
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   CITY: New York, NY FAX #: (212) 997-9880 PHONE #: (212) 835-1400
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FROM: NAME: Thomas C. Mavrakakis, Esq.
DIRECT DIAL NUMBER: (650) 463-8169 USER ID: 5229
NUMBER OF PAGES, INCLUDING COVER: 3 CHARGE NUMBER: 06816.0060.000000

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SUPPLEMENTAL MESSAGE:

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HOWREY SIMON ARNOLD & WHITE HOWREY LLP WHERE LEADERS GO™

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MENLO PARK, CA 94025-3434
PHONE: 650.463.8100 • FAX: 650.463.8400

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5. NAME: _____ COMPANY: _____
   CITY: _____ FAX #: _____ PHONE #: _____

FROM: NAME: Thomas C. Mavrakakis, Esq.

DIRECT DIAL NUMBER: (650) 463-8169 USER ID: 5229

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SUPPLEMENTAL MESSAGE:

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW • Washington, DC 20037-1526
Tel (202) 785-9700 • Fax (202) 887-0689
Writer's Direct Dial: (202)429-2184
E-Mail Address: BrothersK@dsmo.com

March 19, 2004

VIA FACSIMILE AND MAIL
1-650-463-8400

Thomas C. Mavrakakis, Esq.
Howrey Simon Arnold & White
301 Ravenswood Avenue
Menlo Park, CA 94025-3434

Re: Ricoh v. Aeroflex et al.

Dear Thomas:

This letter is in response to your March 16, 2004 letter continuing defendants' baseless allegations of deficiencies in Ricoh's Preliminary Infringement Contentions ("PICs"). As Ricoh has previously explained, and as below, Ricoh's PICs fully meet the requirements of the Patent Local Rules.

Regarding Pat. L.R. 3-1(a), Ricoh's original PICs more than suffice to "crystallize its theory of the case." It is clear from the original PICs that Ricoh contends that the performance by the named defendants of their respective processes for manufacturing ASICs infringes each of process claims 13-17 of the '432 patent. Each claim is separately set forth and analyzed in detail. We fail to see how the original PICs could have been any more clear or unambiguous. The revised PICs were not required under the Rules but, in response to your request, Ricoh decided to voluntarily provide defendants with more information than you were entitled.

Regarding Pat. L.R. 3-1(b) and (c), defendants continue to ignore the fact that Ricoh has not asserted against the defendants all of the claims of the '432 patent. Ricoh has asserted only claims 13-17 of the '432 patent and those claims are directed to a "process," not a product. By asserting these process claims, the Accused Instrumentality is not a software product, but is instead the process performed by the defendants. The original PICs provide in more than sufficient detail Ricoh's reading of these process claims on the accused process of each defendant. Nothing more is required under Pat. L.R. 3-1.

The fact that software tools are used in the practice of parts of the accused process does not convert the Accused Instrumentality from a process to a product. The identification of any Synopsys product in the PICs was voluntarily made by Ricoh in order to provide additional details. There is no requirement to provide the preliminary infringement theories in the excruciating detail you demand. See Network Caching Tech., LLC v. Novell, Inc., No. C-01-2079 VRW, 2003 WL 21699799, *5 (N.D. Cal. March 21, 2003).

As discovery provides further information about the processes used by the defendants, and to the extent that discovery reveals that the defendants are also using other tools to perform steps in the asserted processes of claims 13-17, Ricoh will identify such other tools and additional details regarding the accused processes. We fail to see how the fact that we intend to provide you with additional details as discovery proceeds can be a violation of the Patent Local Rules.

Regarding Pat. L.R. 3-1(d), Ricoh has expressly identified that each element of each asserted claim is literally present and present under the doctrine of equivalents in the Accused Instrumentality. Ricoh's PICs thus comply with Pat. L.R. 3-1(d). The case of Genentech, Inc. v. Amgen, Inc., 289 F.3d 761 (Fed. Cir. 2002), that you cite on this issue does not support your position. Unlike the present case, the patentee in Genentech failed to put the accused party on notice in its claim charts that it was alleging infringement by the doctrine of equivalents, but late in the litigation, attempted to allege infringement by equivalents at the summary judgment stage. Here, Ricoh has provided notice of its assertion of both literal infringement and infringement under the doctrine of equivalents well in advance of even the Case Management Conference. Ricoh's original PICs more than suffice to meet the requirements of Pat. L.R. 3-1(d).

Regarding Pat. L.R. 3-1(f), Ricoh has identified certain instrumentalities to preserve its right to rely on them (for any purpose): use of early implementations and variations of the KBSC system; and Ricoh's use in its process of manufacturing ASICs using Synopsys products such as Design Compiler (or variation, e.g., DC Ultra, DC Expert, DC Expert Plus, etc.), DFT Compiler, Prime Time, HDL Compiler for Verilog, Astro, Astro-Rail, and Astro-Xtalk. These processes may incorporate or otherwise reflect claims 13-17 of the '432 patent.

Your letter continues to assert a claim of "waiver" imposed on Ricoh for failing to provide the identifications set forth in Pat. L.R. 3-1(f) and 3-2. We deny that any failure of identification took place. Moreover, we note that any purported failure

was cured within days of the submission of the original PICs, and well within the deadline imposed by the Patent Local Rules (i.e., "not later than 10 days after the Initial Case Management Conference," Pat. L.R. 3-1). The sanction of "waiver" or exclusion based on such "alleged discovery violations are generally improper absent undue prejudice to the opposing side." Amersham Pharmacia Biotech, Inc. v. Perkin-Elmer Corp., 190 F.R.D. 644, (N.D. Cal. 2000) (citing Wendt v. Host Int'l, Inc., 125 F.3d 806, 814 (9th Cir. 1997)). Clearly defendants cannot show any prejudice, let alone "undue prejudice," and indeed you have not even claimed to have suffered any form of prejudice.[1]

The date for service of the Defendants' invalidity contentions may be calculated based on our March 12 service date of the amended preliminary infringement contentions. Pursuant to Patent Local Rules, defendants are required to provide their invalidity disclosures no later than April 26, 2004. This morning you telephoned me to request an indefinite postponement of defendants' obligation to serve their invalidity contentions, and Ricoh declines to do so. Alternatively, you requested Ricoh's agreement to an expedited briefing schedule on a motion for relief that the defendants are contemplating. Ricoh also declines that request, especially because we do not know the nature of the relief that defendants may seek. For example, you have previously threatened to seek dismissal of Ricoh's complaint, and Ricoh should be entitled to the full amount of time to respond to such a potentially dispositive motion. Although Ricoh believes that any such motion is simply another delaying tactic, once we receive and review the motion, we would be pleased to tell you whether we could agree to an expedited briefing schedule.

Finally, if defendants do proceed with any motion relating to the PICs, as you have threatened to do, we request that you submit a copy of this letter to the Court with such motion.

Very truly yours,

Kenneth W. Brothers

[1] In your letter of March 12, you claim that, by my declining to engage you in a war of words with respect to some of your unsupported accusations, Ricoh has purportedly tacitly admitted that its infringement claims are either insufficient or limited. As stated in my letter of March 12 and reiterated here, Ricoh does not agree.

FAX TRANSMISSION

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP

2004 MAR 19 PM 3:20

DATE: March 19, 2004

CLIENT NO.: R2180.0171

MESSAGE TO: Thomas C. Mavrakakis

COMPANY: Howrey Simon Arnold & White

FAX NUMBER: (650) 463-8400

PHONE: (650) 463-8100

FROM: Kenneth W. Brothers

PHONE: (202) 429-2184

PAGES (Including Cover Sheet): 4 **HARD COPY TO FOLLOW:** X YES ____ NO

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Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 147674)
Erik K. Moller (SBN 177927)
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301 Ravenswood Avenue
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Attorneys for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiffs, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.	Case No. CV 03-04669 MJJ(EMC) **MANUAL FILING NOTIFICATION** **RE EXHIBIT Q TO DECLARATION OF ERIK K. MOLLER IN SUPPORT OF DEFENDANTS' MOTION TO STRIKE PLAINTIFF'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS**

MANUAL FILING NOTIFICATION

Regarding: *Exhibit Q to Declaration of Erik K. Moller in Support of Defendants' Motion To Strike Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions.*

This filing is in paper or physical form only, and is being maintained in the case file in the Clerk's office.

If you are a participant in this case, this filing will be served in hard-copy shortly.

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___ Other (description): _____

Dated: March 30, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Erik K. Moller
Erik K. Moller
Attorneys for Defendants
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL COPR. and MATROX TECH, INC.

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Electronic Engineering Times

Monday, February 6, 1989

Issue: 524

524PG81

Designers moving toward high-level logic representation via logic synthesis
--
Logic synthesis edging up design hierarchy

RAY WEISS

The party is over for gate-level design. Logic designers are moving away from working with the traditional staggered layers of gates and SSI/MSI functions to higher-level logic representations. Today's board-level designers, the logic-design majority, have turned to programmable logic devices (PLDs), instead of gates, to build, control and glue logic. At the same time, VLSI designers are turning to higher-level forms to cope with higher densities and more sophisticated circuits.

Lighting a fire to these developments is logic synthesis. Through it, higher-level logic representations can be mapped into intermediate, implementation-ready forms. And that, simply put, is helping to change the design universe.

The long-range goal for CAE is that of full-scale design synthesis-the implementation of a hardware (and maybe software) design from a high-level, behavioral set of requirements and specifications. Many classes of digital design, such as digital signal processing, peripheral controllers and process control, can be described by such behavioral means. Instead of building systems up from general-purpose blocks, such as microprocessors and controllers, systems can be tailored to meet software or system requirements.

Industry pundit Andy Rappaport, president of Technology Research Group (Boston, Mass.), believes that the future may divide design and synthesis into two distinct forms: one for more standard structures, defined by structures and behavior, and one for building structures from behavioral representations. Today's computers and microcontrollers fit the first description, while specialized DSP and control applications ape the second.

So far, however, it hasn't been a tumultuous revolution. Instead, bit by bit, engineers have shifted to using higher-level forms of logic representation. Insidiously, CAE-long thought the province of those few souls using VLSI-has inserted itself into the design cycle. CAE-with simulation-is now in most digital design

quivers in the form of PLD design-and-burn tools. Engineers are using equations, ABEL-like languages or state machine specifications to specify their PLD-based logic designs.

At the same time, standalone logic synthesis tools are emerging-tools that allow designers to work above the gate level. Not only can engineers work with logic equations, truth tables and state machine forms, but they can now use even higher-level languages for specifying gate-array and standard-cell designs. Hardware description languages, such as VHDL and Verilog, are emerging as drivers for logic synthesis systems. Designs represented in subsets of these languages will be directly converted into net-lists, ready for layout.

Not a new game

Logic synthesis, many experts note, is not a newcomer to the chip game. Silicon compilation, for example, uses logic synthesis to convert high-level descriptions-some behavioral-into intermediate forms, ready for layout. In fact, some of the silicon compiler houses are preparing to provide their logic synthesizers as front-end, stand alone tools.

Synthesis gives VLSI designers more freedom of action. It improves implementation turnaround, enabling them to explore their design space with different speed and real-estate constraints. Additionally, synthesis gives designers working at the gate level the ability to build generic designs-circuits based on a small set of generic functions or cells that are then optimized to take advantage of the foundry library. In addition, register scan-level test functions can be automatically built into a design. SilcSyn, a stand alone synthesis tool, will insert scan-level test functionality into a high-level design description before it is synthesized.

And synthesis provides the missing link between high-level design representations and actual implementations. Without logic synthesis, such descriptions were limited in their usefulness; they had to be hand-converted into lower-level descriptions or implementations. Logic synthesis is rapidly becoming the key to the acceptance and usefulness of the emerging VHDL hardware-description language. Stand alone, synthesis-tool vendors are working to provide VHDL interfaces to convert VHDL descriptions into logic implementations. "Without good tools," noted Rappaport, "VHDL won't really get anywhere."

Rappaport projects that logic synthesis will become a key driving technology for the EDA marketplace. "It is a technology which is needed to raise the level of design." Currently, standalone synthesis tools are about 2 percent of the overall market, at $19.8 million. However, this is expected to rise rapidly, to $265 million by 1992, taking over 9 percent of the EDA software market. This

projection includes the front-end synthesis tools from silicon compilers as well.

The First Born-PLDs

Logic synthesis allows engineers to define the circuit functionality at an equational level. Thus, programmable logic devices have become a prime target for logic synthesis. More designers have embarked on the synthesis road by using what is becoming an industry standard-Data I/O's ABEL-as an easy-to-use form to describe combinatorial logic as well as complex sequential logic.

The Redmond, Wash.-based company also supports state machine descriptions. Circuits defined in an ABEL representation are converted by synthesis to JEDEC-specified fuse maps for burning into the chips. The software minimizes and optimizes the circuit as well, fitting the design into a PLD.

The bad old days, in which an engineer had to partition his or her design and then singly build each PLD circuit, is now over. Software now allows them to partition the design and build it into a number of different PLDs. For example, Data I/O's Gates software package allows engineers to interactively partition their design among multiple PLDs. The design is synthesized from an ABEL-like language and can be simulated with a number of simulators. Unlike earlier PLD design packages, Gates runs on a number of platforms including the IBM

PC AT/386 compatibles, the IBM PS-2, Sun workstations and the Macintosh II.

PLDs have recently been encroaching upon the world of discrete lC logic design. Many systems no longer use discrete circuits-the new Apollo DN10000, for example, uses only VLSI and PLDs. And with PLDs has come the move to higher-level logic representations, as well as the logic synthesis needed to map the equations and state machine descriptions into the PLD fuse maps and physical representations.

Today's PLDs are reliable and are turning in performance that beats out TTL Fast circuits (less than 7 ns for simple PLDs). Moreover, PLD CAE tools now enable designers to work at higher levels of description using languages such as CUPL, Palasm and PLCompiler.

There are more than 300 distinct architectures today, said Michael Mclure, Data I/O product line manager. He said architectures are a lot
easier to work with than VLSI gate arrays and standard cells and

carry far less risk. "Moreover, there are now sophisticated architectures-PGAs [programmable gate arrays! that give designers high densities with the low NRE of PLDs."

Because of Data I/O's position as the number one PLD burner supplier, Gates supports almost all of the PLDs, including the PGAs. Data I/O is working with Xylinx to build a Gates front end for the RAM-based LCAs. "We intend to support all of the PLDs out there," said Mclure.

Working concurrently with PLD designers are board-level designers. They can have automatic PLD partitioning in their design systems done on the PLDesigner from Minc Inc. (Colorado Springs, Colo.). This tool provides a full-design environment for the PLD design engineer. It supports a sophisticated interface and handles all phases of PLD design from entry, synthesis and JEDEC file generation. The software provides a PLD language-PLDcompiler-that accepts normal logical forms of entry as well as some procedural constructs. In addition, the package accepts waveform entry, which it converts to an equational form for logic synthesis. With it, users can submit the needed output waveforms and the corresponding input waveforms and synthesize a PLD.

PLDesigner will automatically partition a design and map it into user-acceptable PLD components. By restricting the selection of components, processing can be sped up. Moreover, the user can specify timing and chip constraints controlling the partitioning and mapping process. PLDesigner supports most of the popular PLDs. According to Minc, it runs on Apollo, Sun (including the 386i), Intergraph and PC AT workstations. It is compatible as well with Mentor Graphics, Daisy/Cadnetix, Intergraph and Teradyne/Case CAE tools.

Another package that features automatic PLD partitioning and selection is the PLD Design System from the Hewlett-Packard Co. Running on the HP 9000 series 300 workstations, it links into the HP Electronic Design System. The software allows engineers to enter designs through gate-level schematics (or net-lists), waveforms, truth tables or state machine descriptions. It supports hierarchical designs (they don't have to be flattened) as well. The software generates HILO 3 models for system simulation.

And Orcad Inc., the CAE company known for its popular schematic-capture package, also is fielding an interactive PLD development package. This package links into the Orcad simulator, VST and schematic capture system. Orcad has introduced streamlined notation and indexed equations to minimize PLD logic equations.

Synthesis as a tool

Sophisticated synthesis tools have sprung up in the past year to make the job of synthesizing a bit easier. Three sets of tools aimed at the gate array and standard gate markets especially stand out. They are the Logic and Design Consultants from Trimiter (Pittsburgh, Pa.); the Logic and Design Compilers from Synopsys Inc. (Mountain View, Calif.) and SilcSyn from Silc Technologies Inc. (Burlington, Mass.). With them, VLSI logic designers no longer have to work directly with the foundry's macro or cell library: they can work at higher level of abstractions avoiding the detail of gate-level design.

These tools are designed to fit in with existing CAE tools and foundries. Unlike silicon compilers that go down to the layout level, they work at the net-list level. Designs can be input in a higher-level form and are then optimized for user-defined constraints, as well as minimized. The tools output standard net-list forms for integration into the existing CAE design flow.

"Logic synthesizers," said Bob Dahlberg, Synopsys vice president of marketing, "don't have to synthesize the whole chip. Even large chips, 100K gates or above, don't have that large amount of random logic. Most of the chip is taken up with regular structures such as registers and memory. Only a small portion of a design, 20 percent, consists of control logic. Our customers estimate that their engineers spend 80 percent of their time working on that logic." With synthesis, engineers can take portions of their hierarchical chip design and optimize them by trying different design combinations.

"The level of abstraction for logic design had to go up," explained Jeff Fox, Silc vice president of engineering. "Designer efficiencies increase with higher levels of abstraction. It is analogous to abstraction in software where higher-level programming languages increase programmer productivity. Consider machine language equivalent with gates, assembly language with logic equations, interpreters with RTL, compilers to algorithms and operating systems to behavioral."

Surprisingly, two of these vendors tools (Silc and Synopsys) also enable designers to continue to work at the gate level effectively. Engineers can build generic designs-designs using a small subset of popular, easily used macros or standard cells.

"This is a potentially big win for synthesis," said Technology Research Group's Rappaport. "They will no longer have to optimize their designs by finding the right library components to minimize real estate and/or circuit delay."

Instead of spending time searching the library to match circuits,

engineers can let the software do it. The tools will map the existing, generic design into the library elements. This approach gets over one of the biggest hurdles for gate-level ASIC design-large design libraries. When VLSI ASICs emerged, the CAE and foundry vendors supported simple SSI/MSI-level design, the same as for discrete logic ICs like the 5400/7400 TTL chips. However, as the libraries grew, this was no longer effective. For an efficient circuit, especially with layout sensitive CMOS, engineers had to use special macros or cells.

Silc has implemented test synthesis in the SilcSyn tool. Engineers can have register-transfer-level-scan test synthesized directly into their designs at the architectural level. Moreover, the technique implemented by Silc allows designers to specify full or partial scan. With partial scan, developed by Silc synthesis manager Barry Rosales, all registers are not linked into sequential scan chains. Instead, key registers are specified with the others feeding into them to add data to the chain for verification.

The partial-scan technique minimizes the overhead for scan level test. The designer can interactively set scan path goals, trading off coverage, test time and overhead. Rosales claims that typical partial-scan overheads are on the order of 10 to 15 percent, rather than

20 to 30 percent for full scan.

In addition, Silc also has included an automatic-test-pattern generator that provides test patterns for based designs.

Meanwhile, Synopsis's Design Compiler is a rule-based system with multiple knowledge bases; therefore it can easily be extended to handle new input formats or libraries. A special package, the Knowledge Consultant, enables designers to build the special knowledge bases for conversions. The Knowledge Consultant uses an OPS 5-like inference engine to select and fire the rules that make up the databases.

The Design Compiler supports rule-based parameterized synthesizers that can generate optimized blocks for synthesizable functions like adders, multipliers, shifters and datapaths. Additionally, it keeps track of previously synthesized functions over a period of time and uses them as needed.

As noted earlier, logic-synthesis maps designs that are described in a high-level hardware-description language (HDL) into a lower-level logic or implementation form. Using an HDL makes the design technology-and even component-independent. Thus, designs can be evaluated functionally without the overhead and complexity of

actual circuits. Moreover, a design can be specified in an evaluatable form that can be used to verify the final implementation.

Silc Technologies Inc. defined their own behavioral/structural language, Design Description Language (DDL), for the SilcSyn synthesis tool. DDL is a simple but powerful language and is a descendant of the pioneering MIT MacPitts synthesis system.

Loosely based on a Lisp format, SilcSyn allows a user to define a design as a series of separate combinatorial and sequential machines. It also includes procedural constructs for limited behavioral definitions. Users can build designs with multiple clocks, synchronous and asynchronous. The software also has a built-in protocol for communications between different clocks.

In operation, SilcSyn first synthesizes the design at the architectural level with state minimization and micro-architectural optimization to share resources such as datapaths, adders and registers. This enables designers to specify a design loosely, letting the system do the work of finding common conditions and sharing components. The design can be functionally simulated for correctness at this level.

SilcSyn then passes the micro-architecturally optimized design through its builder synthesizer. The builder synthesizer optimizes the design, mapping it into the target foundry library (it first maps into a generic design, then into the specific library elements). Currently, SilcSyn works with NCR, SMC, LSI Logic, Fujitsu and Toshiba libraries.

Synopsys has taken another HDL tack: instead of developing a proprietary HDL, Synopsys programmers designed an interface to Verilog, the highly popular HDL from Gateway Design Automation Corp. (Westford, Mass.).

The Synopsys Design Compiler takes Verilog input and synthesizes logic from it. It does not support the full language, particularly the development environment control operators or some behavioral constructs. But designers used to Verilog can now have portions of their existing designs synthesized directly into logic.

Meanwhile, Trimeter's Design Consultant, the company's next-generation synthesis package, is now in beta test and is expected out in the first half of the new year. It accepts VHDL-the VHSIC hardware-description language-Netlist, state machine and Boolean equations, and PLA formats as inputs. Henry Alword, Trimiter marketing manger, said the new package will be the first commercial VHDL synthesis package to synthesize a subset of the VHDL

language. In general, VHDL is gaining in importance in the synthesis community. Silc, Synopsys and Trimiter have all announced intentions of providing a VHDL front end to their synthesizers. This would allow VHDL descriptions to be synthesized into logic.

However, there is a problem in that VHDL was designed for logic description-not synthesis. And portions of VHDL are just not synthesizable. So the industry is working to define subsets of VHDL for synthesis. Silc is working with Vantage Analysis Systems Inc. to provide a VHDL front end to SilcSyn. And Synopsys has developed a general front end for HDLs, including VHDL.

Exploring the design space

An unfortunate fact of engineering life is that old designs just don't fade away. Much of a designer's life is spent reworking or interfacing into existing logic circuits. Additionally, existing logic is moved to new, more efficient (faster and smaller) technologies: from discretes to VLSI, from gate arrays to standard cells, or from one gate-array technology to another.

Synopsys set out to accommodate these design migrations. The Logic Compiler and Design Compiler take in existing circuits as netlists. They can then be remapped into a selected foundry library.

"The engineer can explore the design space," explained Synopsys architect Aart de Geus. "We allow him to specify various timing and space constraints and see the effect on the actual design at the schematic level."

Critical path circuits can be varied by taking different design approaches, all paying careful attention to timing to ensure performance. The Design Compiler works with libraries from Fujitsu, Harris, LSI Logic, National, NEC and Toshiba.

"Design always involves trade-offs," noted de Geus, "but until now the feedback was delayed. You had to try to optimize your design and minimize time and real estate, while varying parameters to try and get the best mix."

Synopsys claims that logic synthesis on customer circuits has delivered both speed and real estate improvements. On the average, according to Dahlberg, circuits showed a 31 percent speed improvement and a 24.4 percent improvement in area optimization. Logic synthesis doesn't deliver order of magnitude improvements-what it does do is ease the implementation task while allowing the designer to better fit the design into the technology.

With SilcSyn, designers work at a micro-architectural level. "They can select component design architectures, depending on the design constraints,

said Silc's Jeff Fox. "For example, they can change adder structures depending on the speed constraint going from a ripple through adder to a carry-look-ahead approach."

PLD synthesis II

Another potential big win for standalone synthesis tools is PLD conversions to VLSI. Trimiter has targeted PLD conversion as one way for designers to take advantage of synthesis for existing board-level designs. Many of these designers do not use board-level simulation for their design verification.

Instead, they breadboard the boards using PLDs and then convert the PLD glue logic and control into VLSI gate arrays when the design is checked out. This avoids modeling problems for new microprocessors and control chips. The Trimiter Logic Consultant is being used to convert combinatorial PLAs (simple PLDs) into gate-level ASICs.

Texas Instruments is working with the Logic Compiler, building up knowledge bases for the TI TSC500 1-micron, CMOS standard-cell family and the 1-micron, CMOS gate array family. TI design centers are already using Logic Consultant to convert PLDs into gate arrays. According to TI, the tool has proved invaluable for PLA-to-VLSI conversion. Generally, about 50 gates can handle a simple PLA, leaving room for more than 140 PLAs on a 8,000K gate array. Design conversion times are minimal; one design with 10 10-ns PLAs was converted in four hours, compared to the three to five days normally associated with each PLA for hand conversion.

In addition, TI is building a third knowledge base to accommodate their bipolar and ECL gate arrays. Using Logic Consultant, engineers will be able to easily map their designs across different design implemtations-gate array or standard cell, as well as across different technologies-CMOS or bipolar. PLA breadboards can be migrated into a range of PLA solutions giving designers the freedom of performance and sizing options.

Logic Consultant only handles combinatorial logic; however, the new Design Consultant supports both sequential and combinatorial logic. With it, designers will be able to convert registered PLDs, including those with buried registers and counters into gate-array

macros or standard-cell logic.

PLD migration is also supported by VLSI Technology Inc. (San Jose, Calif.), a combination foundry and silicon compiler house. The VTI State Machine compiler supports PLA structures, both VLSI and discrete. It can be used to define breadboard PLDs, which can then be converted into VLSI.

Compilers

Silicon compilers have always been part and parcel of logic synthesis. Typically, silicon compilers are made up of a set of specialty compilers-software that maps designs directly into an physical implementation form complete with masks. Module compilers include RAM, ROM, general logic and random logic-block compilers. Synthesis may consist of multiple steps, each mapping to a lower-level representation, eventually reaching transistor mask level.

Silicon compilers partition the problem by providing different compilers for different structures, said Misha Burich, vice president of engineering at Silicon Compiler Systems Inc. (San Jose, Calif.). He said that silicon compilation can be viewed as two separate synthesis processes: logic synthesis and layout. And unlike the standalone synthesizers, the module generators or block compilers handle layout as well. Thus, they provide tight integration with logic synthesis, including back annotation for layout-generated timing.

Silicon compilation is no longer strictly tied to a single foundry, Bindra observed, noting that Silicon Compiler Systems has relations with more than 30 foundries. "We get two kinds of customers, system and board designers, and chip houses such as Motorola, who did the 88000 chip set with our tools," he said.

Motorola plans to use silicon compilation to build variants of the 88000 chip set, adding functional units to the RISC processor design for specific application areas.

To Mick O'Brian, VTI product marketing manager, a chip is not a monolithic logic element. Silicon compilation provides "logic design by compiler," O'Brian said. Designers must partition their design into the major blocks and then use the requisite compiler to build up their designs. The VTI compiler stable includes Logic Synthesis (State Machine), DataPath, RAM/ROM/PLA/MPX and standard-cell compilers. VTI can also synthesize in test.

The separate block compilers give the designer different methods and technology to apply to a given problem. VLSI Technology Inc.'s Logic Synthesizer (the State Machine Compiler with additional features) maps down to a number of physical representations including discrete PLDs, gate arrays, standard cells and custom VLSI. It also provides a transition mechanism to convert discrete PLDs into VLSI, since the PLD descriptions can be mapped to any physical form.

Seattle Silicon has taken a high-level approach to logic synthesis. The new ChipCrafter silicon compiler uses a C-like design language for synthesis of control and random logic. The circuits are synthesized from this description. However, the final circuits are then verified against this high-level description through simulation, ensuring that the high description and final layout forms match.

While most of today's commercial synthesis tools aim at the first class of design forms, one company, JRS Research Laboratories Inc. (Orange, Calif.), has tackled the second-an algorithm/software-driven form of design. This year, the company will be shipping the Integrated Design Automation System (IDAS), a full-synthesis tool set aimed at producing computer architectures based on software metrics. Users can also describe the architecture using a subset of VHDL, which can then be synthesized constrained by the performance characteristics of a set of programs.

IDAS was designed to provide the military with a high-level design tool to produce application-specific embedded processors. "The focus was on performance for specialized applications such as signal processing and
image processing," said Erwin Warshawsky, JRS president. The CAE tool tailors the computer design for optimal application performance. In addition, it gets around the real-time performance problems with Ada by designing Ada-specific architectures. In fact, users can design a microcoded architecture with Ada-generated microcode. That's a real boon, since it eliminates the expensive, tedious process of building processordependent, application-dependent microcode.

Users can specify architectures that IDAS maps into, including VHSIC chip sets and bit-slice architectures. Or the design can be synthesized through the Seattle Silicon silicon compiler.

As a by-product, IDAS produces a processor-specific ADA cross compiler for software development. IDAS is a sophisticated system: It supports Smalltalk/Prolog-based PCs as front ends to VAX servers running an object-oriented database.

---- INDEX REFERENCES ----

INDUSTRY: ELECTRONICS SEMICONDUCTORS INDUSTRIAL TECHNOLOGY (ELQ SEM ITC)

Word Count: 3949

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END OF DOCUMENT

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PATENT 6/A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MJ 4/26/89

H. Kobayashi and M. Shindo
Serial No. 143,821 Group Art Unit 234
Filed: January 13, 1988 Examiner: V. Trans
For: *Knowledge Based Method and Apparatus For Designing Integrated Circuits Using Functional Specifications*

April 18, 1989

Honorable Commissioner of Patents
and Trademarks
Washington, DC 20231

AMENDMENT

Sir:

This Amendment is responsive to the rejection mailed January 18, 1989. The Claims are amended to more clearly distinguish them over the prior art. The Specification, the Summary of the Invention and the Abstract of the Disclosure are likewise amended to clarify the distinction. The objections to the drawings are acknowledged and corrections thereto are forthcoming.

In The Specification:

Page 3 line 6, prior to "functional" please add -- architecture independent --.

Page 3 line 14, prior to "functional" please add -- architecture independent --.

Page 3 line 21, prior to "functional" please add -- architecture independent --.

Page 3 line 21, following "into" please delete "a".

Page 3 line 22, prior to "structural" please add -- an architecture specific --.

Page 6 line 10, prior to "representation" please add -- architecture independent --.

Page 6 line 14, following "rectangle" please add -- or box --.

Page 6 line 19, prior to "integrated" please add -- architecture specific --.

Page 7 line 8, following "at" please delete "a".

Page 7 line 9, prior to "behavioral" please add -- an architecture independent functional (--.

Page 7 line 9, following "behavioral" please add --) --.

In The Claims:

Please amend the Claims as follows:

1. (Amended) A computer-aided design system for designing an application specific integrated circuit directly from architecture independent functional specifications for the integrated circuit, comprising

input means operable by a user for defining architecture independent functional specifications for the integrated circuit, and

computer operated means for translating the functional specifications into [a] an architecture specific structural level definition of an integrated circuit.

2. (Amended) The system as defined in Claim 1 wherein said architecture independent functional

specifications are comprised of a series of actions and conditions and wherein said structural level definition [are] is comprised of architecture specific blocks and interconnections between blocks.

5. (Amended) A computer-aided design system for designing an application specific integrated circuit directly from architecture independent functional specifications for the integrated circuit, comprising

a macro library defining a set of [possible] architecture independent operations comprised of actions and conditions;

input specification means operable by a user for defining architecture independent functional specifications for the integrated circuit, said functional specifications being comprised of a series of operations comprised of actions and conditions, said input specification means including means to permit the user to specify for each [action or condition in the defined series of actions and conditions] operation a macro selected from said macro library;

a cell library defining a set of available integrated circuit hardware cells for performing the available operations defined in said macro library [actions and conditions]; and

cell selection means for selecting from said cell library for each macro specified by said input specification means, appropriate hardware cells for performing the operation [action or condition] defined by the specified macro.

Claim 7 line 2, prior to "means" please add -- specification --.

Claim 9 line 2, prior to "means" please add -- specification --.

15. (Amended) A computer-aided design system for designing an application specific integrated circuit directly from a flowchart defining [the] architecture independent functional requirements of the integrated circuit, comprising

a macro library defining a set of [possible] architecture independent operations comprised of actions and conditions;

flowchart editor means operable by a user for creating a flowchart having elements representing said architecture independent operations [actions and conditions];

said flowchart editor means including macro specification means for permitting the user to specify for each [action or condition] operation represented in the flowchart a macro selected from said macro library;

a cell library defining a set of available integrated circuit hardware cells for performing the available operations defined in said macro library [actions and conditions];

cell selection means for selecting from said cell library for each specified macro, appropriate hardware

cells for performing the operation [action or condition] defined by the specified macro; and

data path generator means cooperating with said cell selection means for generating data paths for the hardware cells selected by said cell selector means.

11. (Amended) A computer-aided design system for designing an application specific integrated circuit directly from a flowchart defining [the] architecture independent functional requirements of the integrated circuit, comprising

flowchart editor means operable by a user for creating a flowchart having boxes representing architecture independent actions, diamonds representing architecture independent conditions, and lines with arrows representing transitions between actions and conditions and including means for specifying for each box or diamond, a particular action or condition to be performed;

a cell library defining a set of available integrated circuit hardware cells for performing actions and conditions;

a knowledge base containing rules for selecting hardware cells from said cell library and for generating data and control paths for hardware cells; and

expert system means operable with said knowledge base for translating the flowchart defined by said flowchart editor means into a netlist defining the necessary hardware cells and data and control paths required in an integrated circuit having the specified functional requirements.

20. (Amended) A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising

storing a set of definitions of [possible] architecture independent actions and conditions;

storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set;

describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions;

specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed; and

selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit.

27. (Amended) A knowledge based design process for designing an application specific integrated circuit which will perform a desired function comprising

storing in a macro library a set of macros defining [possible] architecture independent actions and conditions;

storing in a cell library a set of available integrated circuit hardware cells for performing the actions and conditions;

storing in a knowledge base a set of rules for selecting hardware cells from said cell library to perform the actions and conditions defined by the stored macros;

describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions which carry out the function to be performed by the integrated circuit;

specifying for each [describing] described action and condition of said series a macro selected from the macro library which corresponds to the action or condition; and

applying rules of said knowledge base to the specified macros to select from said cell library the hardware cells required for performing the desired function of the application specific integrated circuit.

Claim 28 line 3, preceding "actions" please add -- architecture independent --.

In The Abstract Of The Disclosure:

Please amend the Abstract of the Disclosure as follows:

Page 38 line 4, prior to "functional" please add -- architecture independent --.

Page 38 line 6, prior to "functional" please add -- architecture independent --.

Page 38 line 8, prior to "functional" please add -- architecture independent --.

Page 38 line 9, prior to "functional" please add

-- architecture independent --.

Remarks

The present invention is a computer-aided design system and method whereby the user can design application specific integrated circuits at an architecture independent functional behavioral level. By designing at this specification level, the user need not possess the specialized expert knowledge of a highly skilled VLSI design engineer. The architecture independent functional specification of the desired application specific integrated circuit is preferably defined in a flowchart format. The functional level specification is translated by the system into an architecture specific structural level definition which in turn can be used directly to produce the application specific integrated circuit. The definition at the structural level includes a list of integrated circuit hardware cells selected from a cell library needed to achieve the functional specifications. Data paths among the selected hardware cells are also generated by the system. In addition, the system generates a controller and control paths for the selected cells. The preferred embodiment of the system and method for accomplishing translation from an architecture independent functional specification level to a hardware dependent physical layout level is accomplished by a knowledge base utilizing artificial intelligence and expert systems technology. By so doing, the system synthesizes a design logic as it is being translated.

The Examiner has rejected Claims 1-30 under 35 U.S.C. § 103 as being unpatentable over Darringer et al. (U.S. Patent No. 4,703,435). It is respectfully submitted that based upon the Darringer reference, the present invention would not be obvious to one skilled in the art. Although Darringer et al. does disclose a method and system for automatic logic design and it is known in the art of automatic layout to utilize cell libraries of circuit components, Darringer does not teach the present invention. A very clear distinction between Darringer and the present invention is that the input to the Darringer system is in the form of a register transfer level flowchart control language. Darringer et al., U.S. Patent No. 4,703,435, column 4, lines 26-32. In order for a designer to utilize the Darringer system, he/she must possess a sophisticated understanding of the complexities of the circuit logic itself and therefore have the specialized expert knowledge of a highly skilled VLSI design engineer. In contrast, the application specific circuit designer utilizing the present invention need not possess any expertise common among highly skilled VLSI design engineers since input to the present invention is in the form of an architecture independent functional specification.

While Darringer may synthesize logic from a register transfer level flowchart description, it provides no knowledge base of any kind. In contrast, the present invention, as defined in Claims 6, 11, 16, 18, 21, 23, 27 and 29 for example, provides a knowledge base in the form of a rule based automatic logic synthesis component, i.e. an expert system. Thus, Darringer does not teach the method of

synthesis utilized by the present invention. Furthermore, although it is known in the art of automatic layout to utilize hardware cell libraries, a rule based expert system has not been utilized to accomplish a task of selection of cells from the cell library. This clearly distinguishes the present invention over Darringer et al.

Although Darringer et al. does disclose a type of flowchart editor, it is in the form of a noninteractive, nongraphic editor. In contrast, the present invention, as defined in Claims 3, 5, 7, 8, 9, 15, 18 and 28 for example, consists of a front end interactive graphic interface whereby the user of the editor, i.e. the designer, can interactively add, delete and modify elements representing operations in the form of actions and conditions as well state transitions between these elements. Thus, Darringer et al. also does not teach to one skilled in the art the input device for the present invention.

It follows from the above analysis, that the present invention is clearly patentable over Darringer et al. as a result of the input of a design at an architecture independent functional specification level, a knowledge based synthesis of the design during translation, and the front end interactive graphic interface.

The Examiner, alternatively rejected the present invention as unpatentable over Nash et al., *Front End Graphic Interface To The First Silicon Compiler*, European Conference On Electronic Design Automation (EDA 84), March 26-30, 1984, Conference Publication No. 232, pp. 123-124, in light of Darringer et al. It is respectfully submitted that the present invention is likewise clearly patentable over

this cited combination of references. The designer utilizing the Nash et al. system specifies that the design in a layout level description language that is hardware dependent. Examples of this description language appear at Nash et al., pp. 122-133. As in Darringer et al., the designer must possess some of the specialized expert knowledge of a highly skilled VLSI design engineer. In contrast, a designer utilizing the present invention, defines the design at a architecture independent functional specification level and need not have any of the specialized expert knowledge of a highly skilled VLSI design engineer.

Although the Examiner states that Nash et al. discloses a graphic editor driven by a knowledge base, in reality, this limited utility, if it even can be called such, merely provides on-line help information to flag syntactical errors during the editing phase. In contrast, the present invention, utilizes a knowledge base which consists of a rule based expert system to synthesize logic, i.e. data and control path, from an architecture independent functional flowchart description of the circuit design.

Nash provides a front end graphic interface in the form of an interactive layout editor which allows for operations such as placement of primitives, placement of pads, modification of primitives, and creation of a signal mode. In contrast, the present invention provides an interactive flowchart editor and simulator which permits the user to interactively add, delete and modify operations consisting of actions and conditions as well as state transitions between these operations.

The present invention is clearly patentable over Nash et al. as is evident from the above analysis. Furthermore, the present invention is also clearly patentable over Nash et al. in light of Darringer et al. since neither teach to one skilled in the art an architecture independent functional specification level method for designing integrated circuits or a knowledge base for logical synthesis during translation of the design to a hardware dependent description such as a netlist.

In addition to the Darringer et al. and Nash et al. references, several other references were cited by the Examiner as being relevant to this case. The first such reference is L. Trevillyan, *An Overview Of Logic Synthesis Systems*, 24th ACM/IEEE Design Automation Conference, 1987, pp. 166-172. Trevillyan discusses several logic synthesis systems, one of which is the Flamel system. We have obtained and enclosed herewith a complete copy of the Flamel reference cited by Trevillyan - Trickey, H., *Flamel: A High Level Hardware Compiler*, IEEE Transactions On Computer Aided Design, March 1987, pp. 259-269. Input to the Flamel system is in the form of a behavior specification language defined as a subset of Pascal but is associated with a specified bus architecture where the busses interconnect functional units such as ALUs, adders, registers and I/O pads. Trickey at page 259. As a result, a designer utilizing the Flamel system must possess specialized knowledge of computer architectures. It is not an object of the Flamel system to provide a means for designing application specific integrated circuits where the designer lacks this

architecture sophistication. In contrast, however, this is an object of the present invention.

Three other systems which Trevillyan discusses are the Polaris system, the APLAS system and the LSS system. A user of the Polaris and APLAS systems must possess specialized knowledge of a highly skilled VLSI design engineer relating to computer architecture and hardware since input to the systems is in the form of register transfer level languages. Input to the LSS system is in the form of register transfer level languages and source code level language. Therefore, the user of this system must also possess knowledge of computer architecture and hardware. Furthermore, none of these three systems utilize expert systems to accomplish the task of logic synthesis.

The final system which the Trevillyan reference considers is Socrates. Although Socrates is an expert system, it analyzes a netlist rather than generates netlists. Furthermore, input to the Socrates system is in the form of Boolean equations, single output PLAs, or a netlist at the register transfer level. As a result, a designer utilizing the Socrates system, as in all the other systems considered in the Trevillyan reference, must possess the specialized expert knowledge of computer architecture and hardware. Finally, Trevillyan specifically states at page 171 that even though the "synthesis from algorithms" approach is a goal that everyone would like to reach, it is not really practical yet in a production environment. This further clearly distinguishes all these systems considered by Trevillyan from the present invention and shows that the present invention is clearly patentable over those systems.

The two Friedman et al. references, Friedman, T.D. and Yang, S., *Methods Used In An Automatic Logic Design Generator (Alert)*, IEEE Transactions On Computers, Vol. C-18, No. 7, July 1969, pp. 593-614 and Friedman, T.D. and Yang, S., *Quality Of Designs From An Automatic Logic Generator (Alert)*, 7th Design Automation Conference, 1970, pp. 71-89, were cited by the Examiner. The Alert system disclosed in the Friedman et al. references, however, are clearly distinguishable from the present invention and furthermore, the present invention is not obvious from the teachings of the Friedman et al. references. Input to the Alert system is an architectural description in Iverson where the user must define the instruction set, major registers and data flow paths as well as declare storage, channels, important registers, flip-flops and other physical devices. Furthermore, the user must specify memory size, word length, instruction format and other hardware design features. See Friedman et al., *Methods Used In An Automatic Design Generator*, at page 595; Friedman et al., *Quality Of Designs From An Automatic Logic Generator*, at page 71. It is clear, therefore, that a designer using the Alert system must possess the expert knowledge of a highly skilled VLSI design engineer relating to computer architecture and hardware. In contrast, however, a user designing an application specific integrated circuit with the present invention need not possess such sophistication. Furthermore, the output of the present invention is a netlist whereas the Alert system generates Boolean equations of logic block descriptions.

Darringer, John A. et al., *Experiments In Logic Synthesis*, IEEE, 1980, pp. 234-237a cited by the Examiner in turn cites Parker et al., *The CMU Design Automation System - An Example Of Automated Data Path Design*, Proceedings Of The 16th Design Automation Conference, Las Vegas, Nevada, 1979, pp. 73-80. We have obtained Parker et al. and enclose a complete copy herewith. Input to the CMU design automation system is in the form of an algorithmic description in the ISP language. The behavioral description in ISP is translated to the first level path graph with interconnection of abstract components and is then mapped to the next level of data path graph with physical modules selected. Output from the system uses input to the Sandia design system. Therefore, the CMU design automation system as well as the Parker et al. reference do not teach the present invention to one skilled in the art.

A final group of references cited by the Examiner are two Watanabe et al. U.S. patents, Watanabe et al., U.S. Patent No. 4,651,284 and Watanabe et al. U.S. Patent No. 4,700,317. Although the Watanabe references utilize a knowledge base containing rules for layout planning specifying the geometric location of objects, Watanabe utilizes a netlist rather than generates a netlist. Furthermore, the Watanabe system does not synthesize logic nor is synthesis even an object of the system. Therefore, the present invention would not be obvious to one skilled in the art based on the teaching of the Watanabe references thus making the present invention clearly patentable over the Watanabe references.

Several other references are cited by the Examiner but are not relevant to the present invention. They will however be considered in the interest of completeness. Two of these references are papers by Darringer et al., more specifically, Darringer, John A. et al., *Experiments In Logic Synthesis*, IEEE, 1980, pp. 234-237a and Darringer, John A. et al., *A New Look At Logic Synthesis*, 17th Design Automation Conference, 1980, pp. 543-548. As was the case in Darringer et al. U.S. Patent No. 4,703,435, both of these papers by Darringer et al. disclose that even though the input may be in the form of a functional specification, the designer must possess specialized knowledge of computer architecture and possibly even the lower level hardware in order to utilize the systems described. The Daniel et al. reference, Daniel, Marvin E. et al., *CAD Systems For IC Design*, IEEE Transactions On Computer Aided Design Of Integrated Circuits And Systems, Vol. CAD-1, No. 1, January 1982, pp. 2-12, also requires the designer to have specialized expert knowledge common among highly skilled VLSI design engineers. The input form for the Cheng reference, Cheng, Edmund K., *Verifying Compiled Silicon*, VLSI Design, October 1984, pp. 1-4, is a description of high level architecture. As evident from the discussion on page 2, however, the designer must possess specialized knowledge of at least computer architecture and possibly the lower level hardware. For these reasons, the present invention would not be obvious to one skilled in the art based upon these references and furthermore, the present invention is patentably distinct over these prior art references.

The Examiner also cited several other patents as prior art. Bryant et al., U.S. Patent No. 4,638,442 and Colton et al., Great Britain Patent No. 1,445,914 both require the designer utilizing the systems to possess at least the specialized knowledge of computer architectures and possibly even sophistication of the lower level hardware date logic. Furthermore, Bryant et al. does not provide a knowledge base for synthesis of logic design. For these reasons, the present invention is patentably distinct over Bryant et al. and Colton et al.

Finally, the last two patents cited by the Examiner as prior art were Coleby et al., U.S. Patent No. 4,635,208 and Dunn, U.S. Patent No. 4,656,603. The Coleby reference is concerned with data structures used to link data records containing design information. Although mention of a logical model is made, it is not at the same level as the present invention. Dunn discloses a rule based expert system which utilizes a graphic user interface. However, Dunn does not teach or suggest the specific combination of features of the present invention as defined in the claims.

In view of the amendments and the foregoing remarks, it is submitted that this application is clearly in condition for allowance. Reconsideration by the Examiner and formal notification of the allowance of all claims are respectfully solicited.

Respectfully submitted,

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Raymond O. Linker, Jr.
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April 18, 89
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SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/143,821			

EXAMINER	
TRANS	
ART UNIT	PAPER NUMBER
234	8

DATE MAILED:

EXAMINER INTERVIEW SUMMARY RECORD

All participants (applicant, applicant's representative, PTO personnel):

(1) Mr. R. Licker (3) _____

(2) Ed V. Trans (4) _____

Date of interview Oct 19, 1989

Type: ☐ Telephonic ☑ Personal (copy is given to ☐ applicant ☑ applicant's representative).

Exhibit shown or demonstration conducted: ☐ Yes ☑ No. If yes, brief description: _____

Agreement ☑ was reached with respect to some or all of the claims in question. ☐ was not reached.

Claims discussed: claims 1, 5, 15, 18, 20 and 27

Identification of prior art discussed: Darringer et al. (U.S. Patent 4,703,435).

Description of the general nature of what was agreed to if an agreement was reached, or any other comments: It is agreed that the features "flowchart editor" and "expert system for translating the flowchart into a net list defining the necessary hardware cells of the integrated circuit" are patentable distinct from the reference identified above. Thus, applicant's attorney will amend the claims to include these features.

(A fuller description, if necessary, and a copy of the amendments, if available, which the examiner agreed would render the claims allowable must be attached. Also, where no copy of the amendments which would render the claims allowable is available, a summary thereof must be attached.)

Unless the paragraphs below have been checked to indicate to the contrary, A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION IS NOT WAIVED AND MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW (e.g., items 1–7 on the reverse side of this form). If a response to the last Office action has already been filed, then applicant is given one month from this interview date to provide a statement of the substance of the interview.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview.

☐ Since the examiner's interview summary above (including any attachments) reflects a complete response to each of the objections, rejections and requirements that may be present in the last Office action, and since the claims are now allowable, this completed form is considered to fulfill the response requirements of the last Office action.

Examiner's Signature

PTOL-413 (REV. 1-84)

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PATENT

**RESPONSE UNDER 37 CFR 1.116-
EXPEDITED PROCEDURE**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

H. Kobayashi and M. Shindo
Serial No. 07/143,821
Filed: January 13, 1988
For: *Knowledge Based Method and Apparatus For Designing Integrated Circuits Using Functional Specifications*

Group Art Unit 234
Examiner: V. Trans

Honorable Commissioner of Patents
and Trademarks
Box AF
Washington, DC 20231

November 15, 1989

AMENDMENT UNDER 37 C.F.R. 1.116

Sir:

In response to the Official Action mailed August 15, 1989, please amend as follows:

In The Claims:

Please cancel Claims 1-4.

~~5.~~ (Twice Amended) A computer-aided design system for designing an application specific integrated circuit directly from architecture independent functional specifications for the integrated circuit, comprising

a macro library defining a set of architecture independent operations comprised of actions and conditions;

input specification means operable by a user for defining architecture independent functional specifications for the integrated circuit, said functional specifications being comprised of a series of operations comprised of actions and conditions, said input specification means including means to permit the user to

specify for each operation a macro selected from said macro library;

a cell library defining a set of available integrated circuit hardware cells for performing the available operations defined in said macro library; [and]

cell selection means for selecting from said cell library for each macro specified by said input specification means, appropriate hardware cells for performing the operation defined by the specified macro, said cell selection means comprising an expert system including a knowledge base containing rules for selecting hardware cells from said cell library and inference engine means for selecting appropriate hardware cells from said cell library in accordance with the rules of said knowledge base; and

netlist generator means cooperating with said cell selection means for generating as output from the system a netlist defining the hardware cells which are needed to achieve the functional requirements of the integrated circuit and the connections therebetween.

Please cancel Claims 6 and 13.

Claim 14, line 1, please change "13" to --5--.

~~15.~~ (Twice Amended) A computer-aided design system for designing an application specific integrated circuit directly from a flowchart defining architecture independent functional requirements of the integrated circuit, comprising

a macro library defining a set of architecture independent operations comprised of actions and conditions;

flowchart editor means operable by a user for creating a flowchart having elements representing said architecture independent operations;

said flowchart editor means including macro specification means for permitting the user to specify for each operation represented in the flowchart a macro selected from said macro library;

a cell library defining a set of available integrated circuit hardware cells for performing the available operations defined in said macro library;

cell selection means for selecting from said cell library for each specified macro, appropriate hardware cells for performing the operation defined by the specified macro, said cell selection means comprising an expert system including a knowledge base containing rules for selecting hardware cells from said cell library and inference engine means for selecting appropriate hardware cells from said cell library in accordance with the rules of said knowledge base; and

data path generator means cooperating with said cell selection means for generating data paths for the hardware cells selected by said cell selector means, said data path generator means comprising a knowledge base containing rules for selecting data paths between hardware cells and inference engine means for selecting data paths between hardware cells selected by said cell selection means in accordance with the rules of said knowledge base and the arguments of the specified macros.

Please cancel Claim 16.

13

~~20~~. (Twice Amended) A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising

storing a set of definitions of architecture independent actions and conditions;

storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set;

storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions;

describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions;

specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed; and

selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base and generating for the selected integrated circuit hardware cells, a netlist defining the

hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.

Please cancel Claims 21 and 25.

Claim 26, line 1, please change "25" to --20--.

~~21~~ 18. (Twice Amended) A knowledge based design process for designing an application specific integrated circuit which will perform a desired function comprising

storing in a macro library a set of macros defining architecture independent actions and conditions;

storing in a cell library a set of available integrated circuit hardware cells for performing the actions and conditions;

storing in a knowledge base a set of rules for selecting hardware cells from said cell library to perform the actions and conditions defined by the stored macros;

describing for a proposed application specific integrated circuit a flowchart comprised of elements representing a series of architecture independent actions and conditions which carry out the function to be performed by the integrated circuit;

specifying for each described action and condition of said series a macro selected from the macro library which corresponds to the action or condition; and

applying rules of said knowledge base to the specified macros to select from said cell library the hardware cells required for performing the desired function

of the application specific integrated circuit and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.

Please cancel Claim 28.

Remarks

This Amendment cancels several claims, thereby significantly reducing the number of claims under consideration. In addition, independent Claims 5, 15, 20 and 27 have been amended to more definitively distinguish applicants' invention over the prior art. The amendments which have been made to these claims involve rewriting the claims to incorporate language previously set forth in dependent claims. As such, no new issues are presented and entry of this Amendment is therefore clearly proper. Favorable reconsideration by the Examiner in light of this Amendment and allowance of all claims as now presented are earnestly solicited.

The recent interview with Examiner Vincent Trans is acknowledged with appreciation. During this interview the independent claims of record were reviewed in detail with the Examiner and it was pointed out to the Examiner how the present invention distinguishes over the prior art. The prior art of record was discussed in detail in the previous response and, for sake of brevity, these previous remarks will not be repeated. Suffice it to say that the present invention distinguishes fundamentally over the prior art by

providing a system and method for designing an application specific integrated circuit at an architecture independent functional behavioral level. Thus, it is not necessary for the user to have the specialized expert knowledge of a highly skilled VLSI design engineer. The invention makes use of artificial intelligence technology, i.e. an expert system, to translate the architecture independent functional level specifications into an architecture specific structural level definition which can be used directly to produce the application specific integrated circuit. It was noted that while the Darringer et al. patent refers at some points in the specification to a so called "functional description", it is clear from a complete reading of the patent specification in context that the specifications used by Darringer et al. are not truly at an architecture independent level, but rather are at a lower level which is indeed hardware architecture dependent and defines the system at a "register-transfer" level description. This is quite clear from the description at column 5 beginning at line 27.

During the interview, the Examiner carefully reconsidered the prior art and applicants' claims, and upon reconsideration agreed that certain features as defined in applicants' claims, such as the "flowchart editor" and the "expert system for translating the flowchart into a netlist defining the necessary hardware cells of the integrated circuit" patentably distinguish applicants' invention from the prior art of record, including Darringer et al. 4,703,435. Thus, it was agreed that Claim 18 in its present form, for example, patentably defines applicants' invention over the prior art of record. Thus, Claim 18 (and Claim 19

which is dependent therefrom) should now be in condition for allowance.

By the present Amendment applicants have cancelled Claims 1-4 and have amended the remaining independent claims so as to place them in condition for allowance. Claim 15 for example has been amended to more clearly recite the use in the system of the present invention of a knowledge base and an inference engine for selecting the hardware cells and for generating data paths between hardware cells. It is submitted that the combination of structural features as recited in Claim 15 defines a novel and unobvious departure from the prior art. Accordingly, Claim 15 and dependent Claim 17 should be in condition for allowance.

Claim 27 is directed to the method aspects of applicants' invention. This claim has been amended to recite the utilization of a flowchart and to additionally recite the generation of a netlist defining the hardware cells of the integrated circuit and the interconnection requirements therefor. This claim and Claims 29 and 30 which are dependent therefrom clearly distinguish applicants' invention over the prior art.

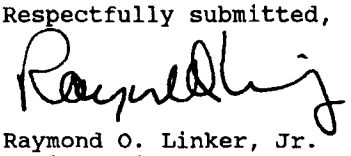
Claim 5 has also been amended to clearly distinguish it over the cited prior art by more clearly defining the expert system aspects of applicants' invention including the provision of a knowledge base containing rules for selecting hardware cells, inference engine means for selecting appropriate hardware cells, and netlist generator means for generating a netlist defining the hardware cells which are needed to perform the functional requirements of the integrated circuit and the connections therebetween. The combination of features as defined in Claim 5 is not

identically shown in any of the cited prior art, and moreover the differences between the invention as defined in this claim and the prior art are quite significant and are not suggested by or obvious from the prior art of record.

Independent Claim 20 has been also amended to emphasize the expert system aspects of applicants' method. Claim 20 as now presented thus defines a combination of method steps which are neither shown nor suggested by the prior art of record.

For the reasons noted it is submitted that all of the claims of the application as now presented are in condition for allowance. Favorable reconsideration by the Examiner, entry of this Amendment, and notification of the allowability of all claims as now presented are earnestly solicited.

Respectfully submitted,



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Date of Signature